28.2 A DC-to-44-GHz 19dB Gain Amplifier in 90nm CMOS Using Capacitive Bandwidth Enhancement

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The design of a CMOS broadband amplifier in 90nm bulk technology, achieving a gain-bandwidth product in excess of 390GHz, is presented. Combined shunt- and series-peaking is employed to increase the BW. To reduce the impact of process variations, a continuously tunable load resistor in the differential-pair stages is used to adjust the gain peaking intensity. Although this variable resistor introduces more parasitic capacitance C_p (Fig. 28.2.1) than a fixed-valued resistor would, it is shown that for a simple shunt-peaking amplifier, this capacitance can be used to enhance BW as much as 20% and reduce group delay (GD) by a factor of 4 within the pass band. The measured BW of the amplifier is 44GHz with 19dB differential gain. The chip dissipates 57mW from a 1.0V supply and occupies 0.02mm^2.

As a starting point for the BW enhancement based on combined shunt- and series-peaking, simple shunt-peaking circuits are analyzed with emphasis on the effect of C_p. Given the supply voltage constraints, the largest tuning range of R_L^* (Fig. 28.2.1) is obtained if R_L^* is connected between V_{DD} and L_P. This R_L-L_P order is the opposite of that commonly found in literature [1, 2, 3]. Equations (1) and (2) are the transfer functions of the circuits in Fig. 28.2.2. If C_p is neglected, they become the same as Eq. (3) that describes simple shunt-peaking. The difference of the 2 topologies is reflected in the first- and second-order terms of the denominators, which implies different pole locations for the 2 circuits. The zeros to which the main BW enhancement is attributed [1, 3] are the same.

$$A_{circuit1}(s) = gm \cdot \frac{s^2 R_L L_P C_p + sL_P + R_L}{s^3 R_L L_P C_L C_p + s^2 (L_P C_L + L_P C_p) + sR_L C_L + 1} \quad (1)$$

$$A_{circuit2}(s) = gm \cdot \frac{s^2 R_L L_P C_p + sL_P + R_L}{s^3 R_L L_P C_L C_p + s^2 L_P C_L + s(R_L C_L + R_L C_p) + 1} \quad (2)$$

$$A(s) = gm \cdot \frac{sL_P + R_L}{s^2 L_P C_L + sR_L C_L + 1} \quad (3)$$

Because neither the GD flatness/ripple nor the 3dB BW of 3rd-order systems are easily accessible by analytical methods, numerical methods are used to find BW and GD optima for the above equations. Figure 28.2.3 shows the relative values of BW, GD, and associated values for m ($m = L_P / R_L^2 C_L$) as a function of the C_p/C_L ratio. Whereas the maximum BW of circuit 1 is independent of C_p, the lowest GD ripple is achieved at $C_p/C_L = 0.4$ and $m = 0.37$ [mark **(A)** in Fig. 28.2.3]. The GD ripple then is 25% of that of circuit 1 with $m = 0.71$ and $C_p = 0$. Thus, while the original BW is preserved, GD is improved, and the inductor size, which is proportional to m, is significantly reduced simultaneously. Compared with circuit 1 with $m = 0.32$ and $C_p = 0$, a GD improvement of a factor of ~5 (~20%) is possible with a 10% increase in BW and a small reduction in inductor size [mark **(B)** in Fig. 28.2.3]. While circuit 2 benefits from an even higher BW enhancement of up to 23%, GD improvements are slightly less and the inductor size reduction is not always positive. Figure 28.2.4 concludes this part of the analysis and shows the magnitude and GD of both circuits over normalized frequency, once for maximum BW and once for lowest GD ripple, in comparison with a non-peaking ($m = 0$) and the classical simple shunt-peaking circuits ($m = 0.32$ and 0.71) [1].

To keep the number of free design-parameters low, the amplifier consists of 5 identical, dc-coupled stages as depicted in Fig. 28.2.1. As soon as the size of the differential pair and of the bias current source are set, their layout is drawn. Based on the layout, the value of the load capacitance C_L of each stage is extracted. Then, using $L_P = mR_L^2 C_L$, the initial value for the shunt-peaking inductor is derived. The initial geometry is found by numerically solving the expression in [4] for the highest "inductance/series resistance" ratio, which, given the manufacturing process metal-width and spacing constraints, results in coils with high self-resonance frequencies. In the following, the layout-extracted schematics and the S-parameters of the coil from full-wave electromagnetic (EM) simulations are used in parametric simulations to adjust the coil parameters and C_p (= physical dimensions of R^*). Once this first optimization step is completed, the series-peaking inductor L_S is introduced. The interconnection path between the individual stages is included in the L_S-EM model. Very few additional iterations are needed to establish the final coil geometries. Figure 28.2.5(a) shows the incremental BW improvements during the design process. It is common practice to absorb the series resistance of L_P into R_L. Therefore small inductors with low quality-factors can be used. This, however, does not hold for L_S: R_S must be kept very low ($R_S = 9.1\Omega$ for this design) to prevent a severe BW degradation. Therefore, L_S is built by tying 2 metal layers together, reducing R_S by a factor of 2. The same technique is applied to the shunt-peaking coil L_P. In this way, the resistive tuning range is increased and, because the inductor must carry a substantial dc current, it complies more easily with electro-migration design rules.

Based on the above analysis and design guidelines, by properly adjusting C_p and using series peaking, a substantial increase in BW compared with simple shunt-peaking is possible (see Fig. 28.2.5). The use of layout-extracted data at the earliest possible stage in the design process and a proper modeling of inductors and interconnects result in a good match between simulations and circuit measurements and in a compact circuit layout. The high gain of the amplifier in conjunction with the variable load resistor allows adjustment of the transfer function over a wide range. Besides of making the circuit immune to manufacturing process variations, this enables a wide variety of new applications, in particular continuous time equalization. Figure 28.2.6 compares this work with similar circuits from the literature, confirming the superiority of the outlined design methodology.

Acknowledgments:
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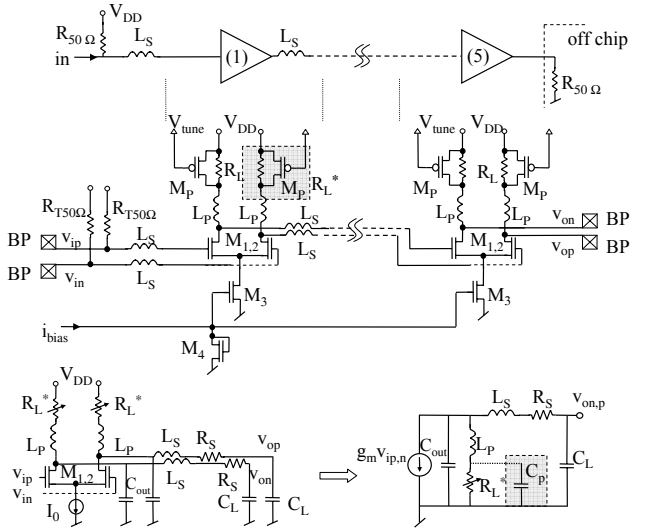
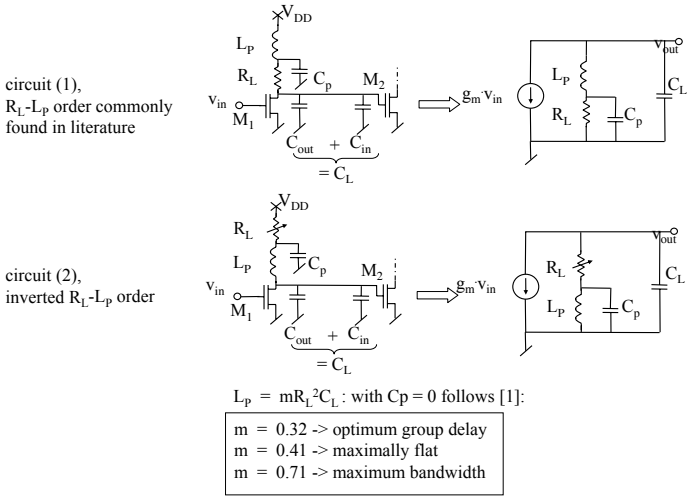


Figure 28.2.1: Amplifier schematics. Top: simplified, middle: detailed, bottom: one stage only with first order parasitics and small signal equivalent.



$L_P = mR_L^2C_L$: with Cp = 0 follows [1]:

m = 0.32 -> optimum group delay
m = 0.41 -> maximally flat
m = 0.71 -> maximum bandwidth

Figure 28.2.2: Common and inverted R_L-L_P order shunt-peaking amplifiers.

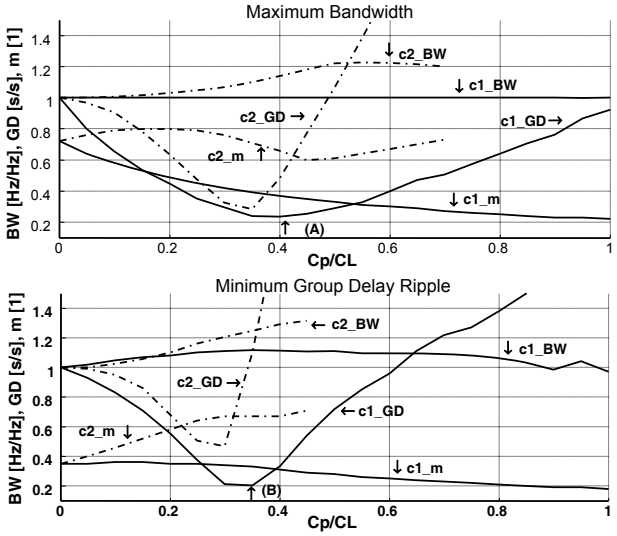


Figure 28.2.3: BW & GD performance as function of C_p/C_L (e.g. c2_BW = bandwidth of circuit 2).

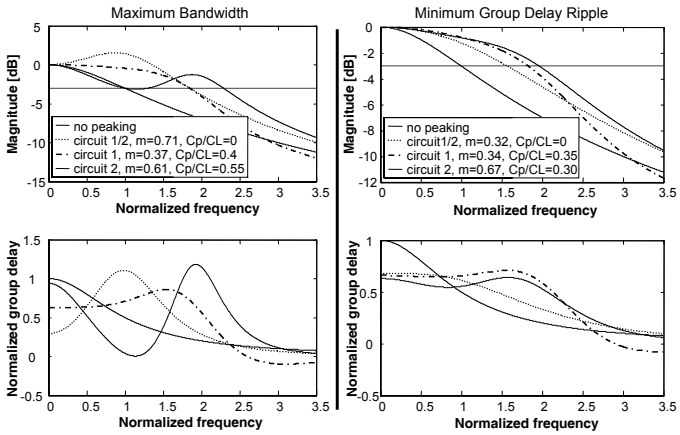
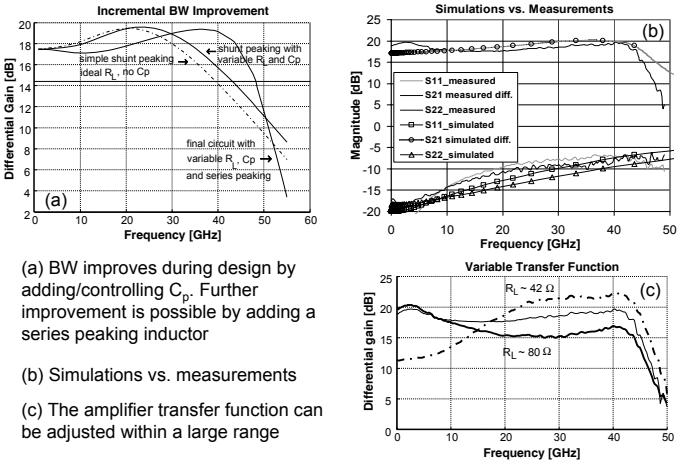


Figure 28.2.4: Frequency responses for different design goals (BW, GD).



(a) BW improves during design by adding/controlling C_p. Further improvement is possible by adding a series peaking inductor

(b) Simulations vs. measurements

(c) The amplifier transfer function can be adjusted within a large range

Figure 28.2.5: Frequency domain simulations & measurements.

Design	Technology	Gain (dB)	BW (GHz)	A_v x BW (GHz)	V_{DD} (V)	Power (mW)
[3]	0.18µm CMOS	15	22	124	2.2	190
[5]	90 nm CMOS	18	23	183	1.2	54
[6]	0.12µm CMOS SOI	9	81	228	2.6	130
This design	90 nm CMOS	19	44	392	1.0	57

Figure 28.2.6: Performance summary and comparison.

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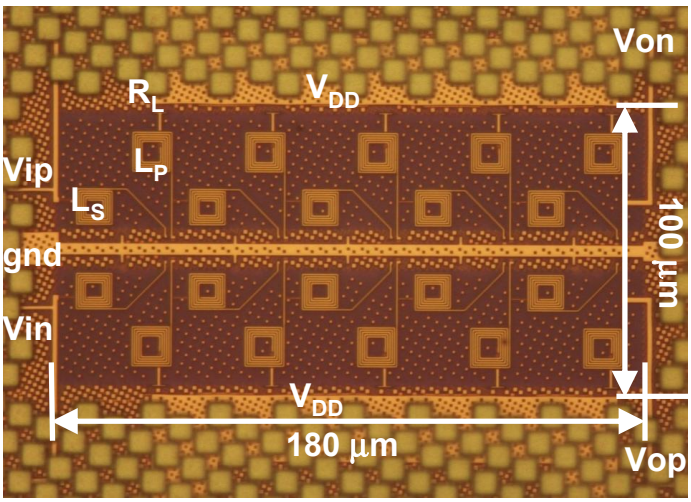

Figure 28.2.7: Chip micrograph.

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